BOSCH PROCESS CHARACTERIZATION FOR DONUT TSV'S

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ABSTRACT
In a continuous quest for cost reduction, the semiconductor industry continues to pursue device scaling techniques. However as scaling becomes more complex and expensive, alternative techniques for cost reduction are being investigated. Progress in 3D packaging (3D-SIC, 3D-SoC) and Interposer technologies have the promise to offer reduced costs and smaller form factors. One of the key features for all of these packaging technologies is Through Silicon Vias (TSV).

In this paper we discuss processing a TSV-Last version of Donut TSV's (DTSV) which are defined by etching a annulus or donut shaped trench in the thinned silicon device wafer using a Bosch etch process. The donut trench is then filled with a polymer that acts as liner and stress buffer. Next, the core of the donut is removed by a self-aligned silicon etching process and filled with electroplated Copper.

There are several challenges arising from the behavior of the Bosch process used to define the donut trench. The first is that the process is sensitive to excessive lateral etching of Si at the PMD (pre-metal dielectric) interface (notching). In order to minimize this effect, the main etching step should stop just before reaching the PMD and the etch should be completed by a soft etch, which produces less defined TSV profiles, is slower than the main etching step and should thus be kept as short as possible. Some over etching is required to account for silicon thickness variation and etch non-uniformity across the wafer.

The second challenge of the Bosch process is Aspect Ratio Dependent Etching (ARDE). For the DTSV's, the aspect ratio is very high and the obtained etch depth will be sensitive to CD variations. The width of the ring in the donut is aggressively small for advanced packaging lithography and tight process control will be required.

In this study the Bosch etch and lithography are characterized and the requirements on the lithography performance are determined. Experimental process windows and lithography modeling are presented on the optimization required to maintain the required CD control. Finally, the optimal etching times for the Bosch process are deduced.

Key words: TSV, Donut TSV, Annulus trench, Via Last, 3D Packaging, Bosch Process

INTRODUCTION
Bandwidth demand and device latency considerations along with power management and distribution concerns have created drivers for new integrated circuit architecture solutions. Semiconductor companies are evaluating the adoption of Through-Silicon Vias (TSV) as a method to achieve interconnect density in the third dimension and reduce long interconnect paths in current planar designs [1]. As the cost of front end semiconductor scaling escalates beyond leading edge technology node, companies are also reviewing the use of TSV as a potential technology for delivering optimal price to performance solution.

The TSV concept appeared in late 1990s and from then on it has been developed and implemented in the IC industry. The TSV is the key element to enable 3D IC integration. TSVs are vertical electrical connections (vias) that pass through a thinned silicon wafer in order to establish an electrical connection from the active side to the backside of the die, thus providing the shortest interconnect path and creating an avenue for the ultimate in 3D integration. TSV technologies offer greater space efficiencies and higher interconnect densities than wire bonding and flip chip stacking. TSVs can be implemented at different stages of the IC fabrication process. In a via-first approach, the TSV is implemented before the Front End of Line transistor modules (FEOL). For the via-middle approach, the TSV is implemented after the FEOL and before the Back End of Line (BEOL) processing. In the case of via-last, the TSV module is implemented after the BEOL and thinning module.

While there are multiple approaches for TSV manufacturing, companies are primarily focusing on via

middle and via last technologies. Manufacturing process flows utilizing via middle approach may affect the electrical and thermal properties of the semiconductor device [2]. To minimize these effects a keep out zone (KOZ) around the TSV is utilized. The KOZ is proportional to the diameter of the TSV which is one of the factors that drive the use of a small diameter TSV. In addition, it is important to maintain sufficient Si thickness to avoid thermal hot spot effects. Together these requirements drive high aspect ratio TSVs resulting in potentially challenging and expensive manufacturing processes. For some device applications the via last approach can offer a cost effective alternative to via middle. This realization is driven by potential cost savings and also by the desire to leverage the existing via last TSV infrastructure currently in use for high volume CMOS image sensor fabrication.

The lithographic study in this paper fits into the implementation of a via-last module using a polymer-isolated, Cu-filled TSV, realized on 50µm thinned wafers bonded on temporary carriers as shown in figure 1 [3]. In this via-last integration scheme, a donut shape trench is etched after thinning of the device wafer to a thickness of 50µm. The target width (**w**) of this trench is equal to 3µm; the inner Si-core diameter of the donut (Ø) will be 5 or 10µm as shown in figure 2(b). This donut shaped trench is, after etch and strip, filled with a polymer material as shown in figure 1(b). This polymer will act as the liner isolation of the Cu-filled TSV, while it is also used as a stress buffer layer (stress induced by the Cu), in order to minimize the KOZ for active CMOS devices.

The donut trench etch has to meet several process integration specific requirements. The first is the deep-Si trench etch needs to stop on a Shallow Trench Isolation (STI) oxide layer because when the STI is reached, excessive lateral etching occurs at the bottom of the TSV. This is known as footing or notching. Figure2 (a) shows a typical pattern for notching of a donut shape trench. Notching would hamper the deposition of a continuous barrier/seed layer and would result in voids during the bottom up electroplating process. Avoiding the notching effect can only be done by modifying the settings of the typical Bosch etch cycle, or Main Etch (ME) [4, 5]. A soft landing etch step (SL) is introduced to eliminate the footing and minimize the notching at the silicon to oxide interface.

The second important process integration requirement is that the deep silicon dry etch process has to be compatible with the total thickness variation (TTV) of the thinned wafers. A typical TTV on 300mm thinned wafers can be 2 to 3µm. The etch depth of the main etch should be selected to just reach the STI oxide in the case of thinnest possible silicon and fastest etch rate. The landing etch should be long enough to guarantee complete opening of the trench.

A third important requirement is the aspect ratio dependent etch rate (ARDE). The deep silicon etch depth will, for a Bosch etch, always be depending on the critical dimension (CD) of the pattern definition by photolithography. In this case the CD is the target width **w**, shown in figure 2(b). There is always a certain variation of CD after lithography and this may influence the performance of the etch process. One of the main purposes of this paper is to investigate this CD variation.

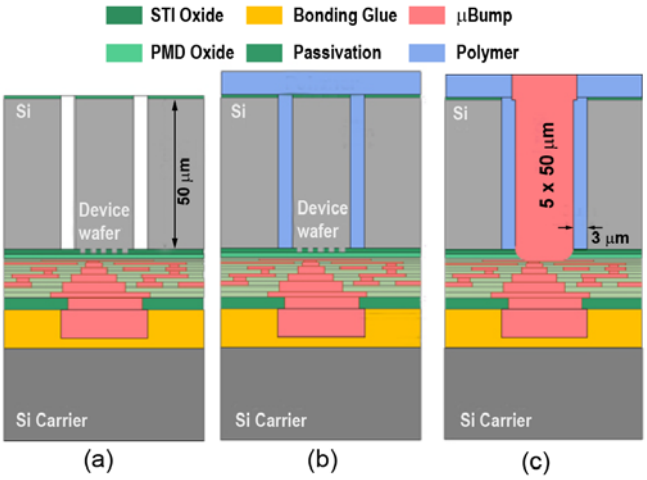

Figure 1: Via last module showing (a) Deep-Si trench, (b) filling the trench with polymer material and (c) TSV after complete via last process module [3].

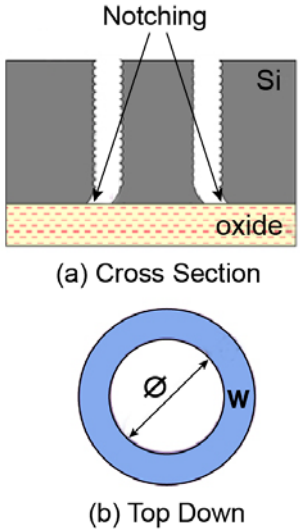

Figure 2: (a) Cross sectional drawing of the Si trench stopping on the STI oxide layer. (b) Top down drawing showing typical core width (Ø) and donut width (**w**).

EXPERIMENTAL METHODS

Equipment

Lithography was performed on an Ultratech AP300 advanced packaging stepper with a 0.16 numerical aperture (NA) Wynne Dyson lens. This unique design permits the use of broadband illumination from a mercury arc lamp, and the system used in this study has a capability to select different wavelengths: i-line, gh-line or ghi-line [6]. Coating and development is performed on a TEL ACT12 Cleantrack. CD measurements are performed on a KLA-Tencor eCD-2.

Etching is performed on an LAM 2300 cluster tool equipped with a Syndion DSiE chamber.

Reticle

Figure 3 shows the lithographic test reticle used in this study. The field consists of a repeating array of test cells. The actual test structures used are an array of isolated linear trenches from 5.0µm down to 1.0µm as shown in figure 3(c).

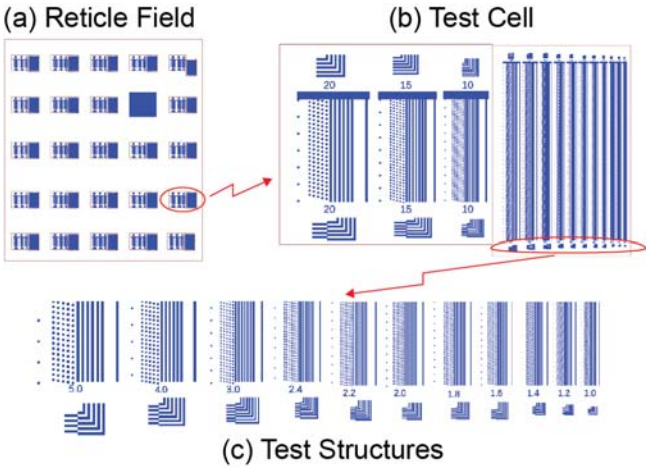

Figure 3: Test reticle layout. The reticle field contains an array of test cells which contain the actual test structures.

Processing

Characterization is performed on Silicon test wafers with 200nm SiN deposition. The photoresist selected is positive tone AZ EM 10XT coated to a thickness of 7.5µm as measured after softbake. Development is performed in a multi puddle process using diluted AZ400k.

First, the process window of the lithographic process is characterized by exposing a focus exposure matrix (FEM) as shown in figure 4. Focus is varied over the X-axis and exposure dose is varied over Y.

To investigate the dependency of etching process on the resist profile, wafers are only exposed with varying focal settings. Exposure variations are not required because the reticle has a large range of line widths defined.

One part of the wafers is subjected only to the main etch and another part is subjected to main- and landing-etch. Analyzing the obtained trenches along the line Y=0 produces data with respect to resist slope. Analyzing along the line X=0 produces within wafer uniformity data. Combined with the known thickness and thickness variation of the thinned wafers, the optimal etching times can be determined.

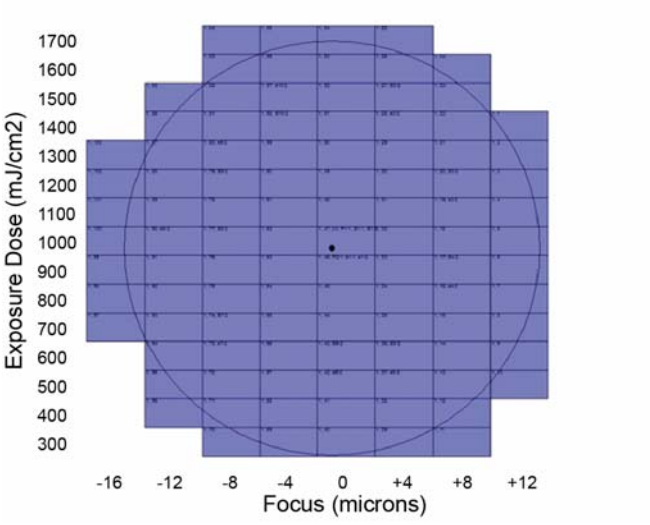

Figure 4: Wafer layout for the FEM. An eight by fifteen array was exposed with focus varying in the horizontal axis and exposure dose varying in the vertical axis.

Analysis

Each array location on the completed FEM wafers were then measured using a top down scanning electron microscope (SEM) to determine the CD at 0% and 100% of the photoresist thickness.

Analysis of TSV profile is performed by cross section SEM. However, the circular characteristic of TSV's or DTSV's makes cleaving unpredictable and reliable analysis of shape and depth is not trivial as is depicted in figure 5(a).

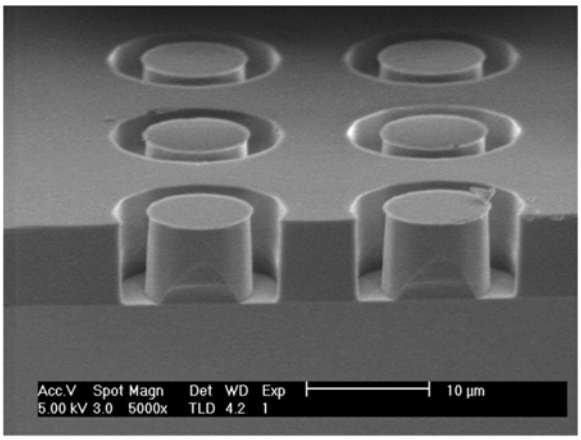

Figure 5(a): Cross-section of 2.4µm Donut TSV's imaged in 7.5µm thick positive photoresist.

Figure 5(b) shows a cross-section of Donut TSV's etched in silicon. The cleave to create the cross-section is not perfectly perpendicular to the surface and it appears that the trenches are much narrower at the bottom which is not the case. To improve the analysis, isolated linear trenches are used as shown in figure 3.

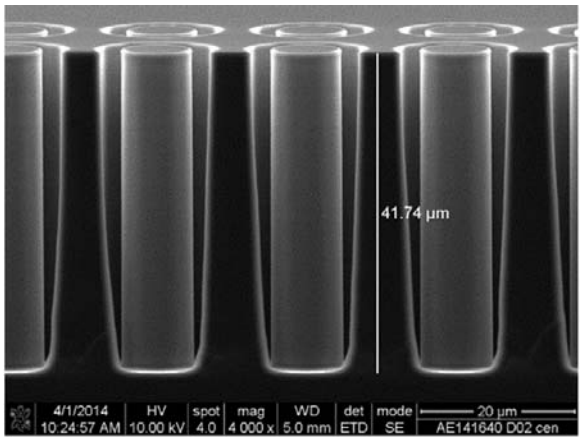

Figure 5(b): Cross-section of Donut TSV's etched in Si. The cleave is not perfectly perpendicular to the surface and it appears that the trenches are much narrower at the bottom which is not the case.

RESULTS AND DISCUSSION

Bossung Plots and Process Windows

In figures 6 and 7, Bossung plots of the focus/exposure matrix (FEM) are shown for the 2.4µm isolated trenches [7]. The focus is varied between -12µm and +12µm and the energy is varied between 600 and 1400 mJ/cm^2. Figure 6 depicts the CD results at the top of the resist pattern and figure 7 depicts the CD at the bottom or foot of the resist profile. The bottom CD is the more critical parameter and lithographic settings are tuned to optimize the performance of this parameter. Observing figure 6 one can see that the sensitivity to energy variation is larger when CD's are at or smaller than the nominal CD. Around nominal there is a range of exposure energies where the dependency on focus is minimal. Selecting an exposure energy that would produce a CD which is 10% larger than designed would produce a more stable process than when aiming at achieving nominal CD.

The top CD is much larger than the bottom CD and is more sensitive to focus variations. The Bossung plot in figure 6 indicates that the optimal focus setting for the top CD has an offset of 3µm.

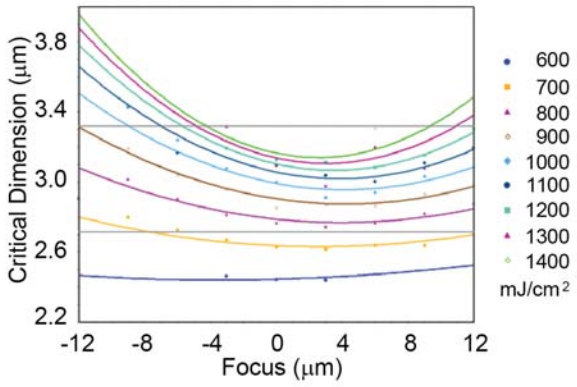

Figure 6: Bossung Plot for top CD 2.4µm linear trenches.

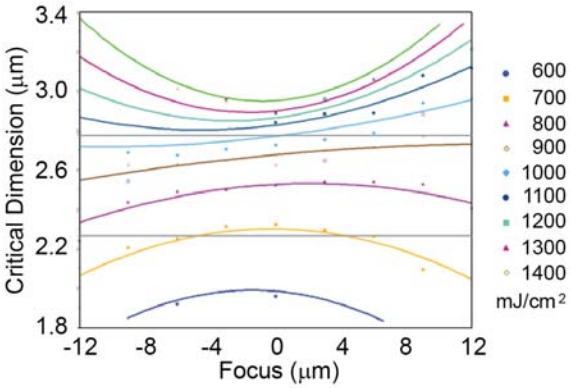

Figure 7: Bossung Plot for bottom 2.4µm linear trenches.

In figure 8 the process window is plotted with the dose on the Y axis and the focus on the X axis. The process window is defined by a typical accepted variation in CD of ± 10% of the target value. In this case the target CD is 2.64µm which equals to 10% sizing. All Exposure/focus combinations that produce a CD on target are drawn in the dotted line. All Exposure/focus combinations that produce a CD that is either 10% bigger or smaller are drawn in the solid blue envelope. The red box is the largest rectangular process window centered on the target CD of 2.64µm. This indicates whether the exposure tool can meet the requirements on focus and energy stability.

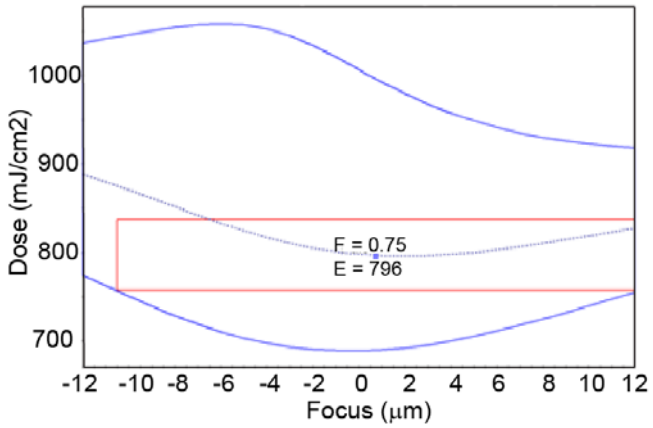

Figure 8: Experimental process window for 2.64µm trenches. The blue curves indicate the ±10% CD limits. The red box is the largest rectangular process window centered at the nominal CD. Sidewall angles are ≥ 86^o as determined by cross sectional SEM.

For the critical 2.4µm design, the process window is much larger than the stability specification of the AP300 wafer stepper. So achieving a stable process is easily achieved.

Uniform wafers were exposed at 800 mJ/cm^2 and 0µm focus. They are measured on every die and show an overall good uniformity with CD = 2409 nm ± 87 nm (3σ). This was also checked on the 3µm structures with CD = 3036 nm ± 77 nm (3σ).

Cross Sectional SEMs

The cross section images of etched trenches at optimal focus, with photoresist still present on the wafer, are shown in figure 9. All images have identical magnification to clearly show the ARDE of the Bosch deep silicon etch. With a CD variation between 2µm to 4µm, the etch depth varies up to 10µm. Although the resist sidewall is not vertical, this is not transferred in the profile of the trench. A small re-entrant effect is visible at the top of the trench. The principle of the Bosch etch process is an alternation of isotropic etching and polymer passivation. Figure 10 shows the top of the trench with the photoresist still present. In the silicon sidewall some notching can be observed which is the result of the alternating etching. The CD at the top of the trench is identical to the original CD as defined after lithography. The polymer should be removed along with the photoresist.

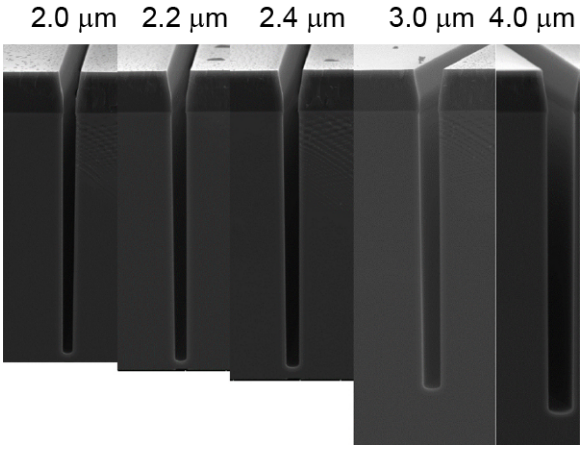

Figure 9: Cross-sections of etched trenches. The CD is of is labeled at the top of each trench. Note that the photoresist has not been removed.

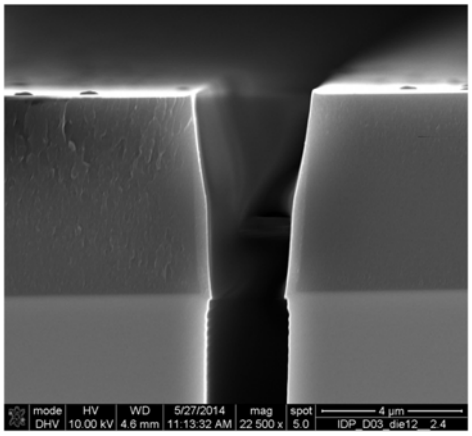

Figure 10: Detail view of the top of an etched trench with the photoresist still present.

The last cross section image in figure 11 shows both the main and the landing etch steps. The latter creates a sidewall that is substantially less straight than with the main etch, as well as a narrower CD at the bottom. However, when landing on STI oxide this process should create much less notching. The etch depth measured across the wafer shows 1.5µm variation peak to peak.

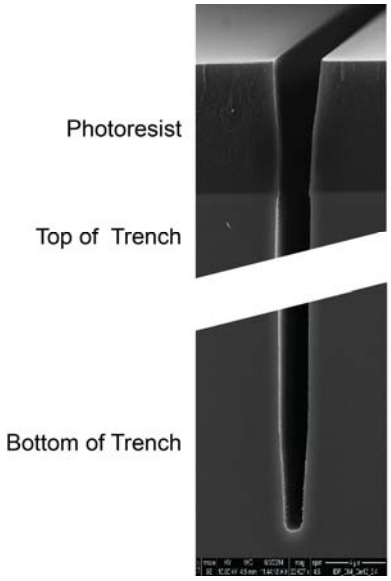

Figure 11: Cross-section of trench after main and landing etch. The landing etch at the bottom of the trench shows a smaller CD and more slope than the main etch at the top of the trench.

Etch Depth Analysis

In figure 12 the etch depth is plotted versus the resist slope. The etch depth was measured along the X axis where the focus was varied, showing a 2µm variation from peak to peak for the 3.0 µm trenches (orange) and 1µm variation for the 2.4µm trenches (blue). This shows that the influence of the resist slope on the etch depth is stronger for structures with a larger CD. In order to keep the etch depth variation limited to 1µm; the slope for 3.0µm trenches is limited to 86°. For 2.4 µm structures the effect on etch depth is almost negligible. For these wafers the focus range was selected from -20µm to +20µm in order to have a larger variation in resist slope. For the CD data as shown in figures 6 and 7 the focus is varied from -12µm to +12µm and within this range the slope is always higher than 86°.

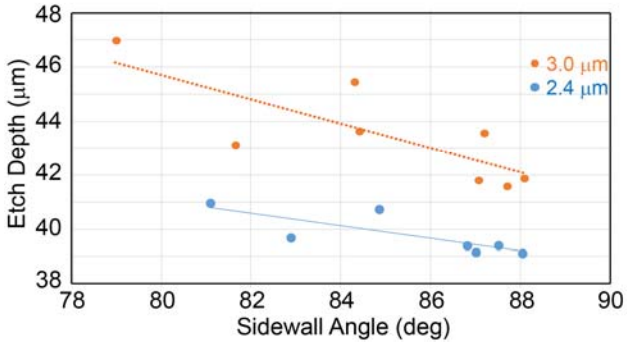

Figure 12: Etch depth dependence on CD and sidewall angle.

The ARDE effect of the Bosch deep silicon etch is shown in figure 13. For a typical lithography process variation of 10% there is a etch depth variation of 1µm for main (blue) and 2µm for main plus landing (orange) for trenches with a 3.0µm CD. The etch variation is 2µm for main and 3µm for main plus landing for trenches with a 2.4µm CD.

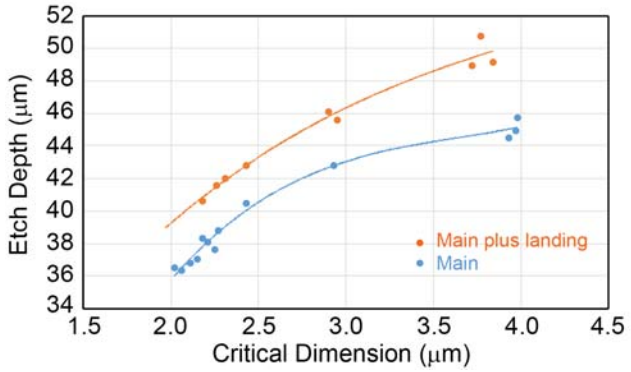

Figure 13: Depth after main etch (blue) and main plus landing etch (orange) versus trench width.

Statistical Process Control Charts

The TTV of thinned wafers after grinding to a thickness of 57µm was evaluated over 4 batches of wafers as shown in Figure 14. Thickness uniformity could be controlled within 2µm total variation. The average thickness per wafer is also controlled within ±2µm.

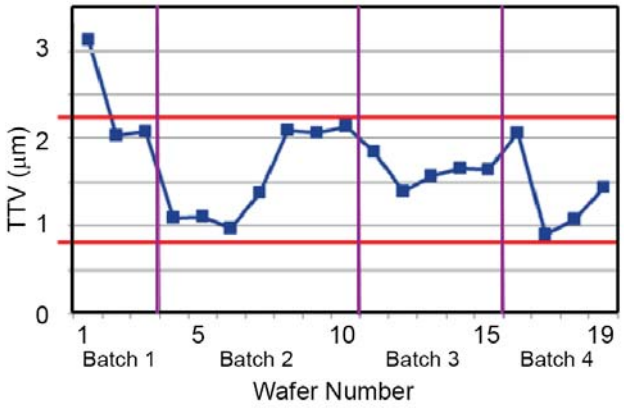

Figure 14: Typical TTV of thinned 300mm wafers for four batches. The red lines show the process control limits.

Etch Depth Calculations

The maximum local thickness error of the thinned wafer is half of the TTV plus the average thickness error. This is 3µm for the process of record. The etch depth that would prevent excessive notching is 50µm minus the square root of the sum of errors squared in thickness, etch uniformity and ARDE effect. For 3.0µm process of record this is:

$$50 - \sqrt{(½ * 1.5)^2 + 1^2 + 3^2} = 46.75\mu m$$

The soft-landing etch has to cover for local thickness variations and the variation in main etch. For 3.0µm process the main etch stops 3.25µm before the target depth of 50µm. Combined with a maximum thickness of 53µm, the landing etch has to add another 6.25µm to the total trench depth. For 2.4µm process, the depth of the main etch is 46.30µm. The landing etch has to add at least 6.7µm.

CONCLUSIONS

Lithographic analysis has shown that process control of donut TSV features down to 2µm is feasible. The process variability is significantly better than ±10% of CD and has the potential to achieve ±5%.

Etch rate variations inherent to plasma etching are 1.5µm peak to peak. The ARDE effect due to CD variation for 3.0µm trenches is 1.0µm. Therefore for a nominal 50µm thick silicon process, the main etch (ME) part cannot be deeper than 46.75µm, while the soft-landing part (SL) should etch at least 6.25 µm deep. In this way, a notch friendly dry etch recipe can cope with incoming wafer thickness, after thinning, ranging from 47µm to 53µm.

From a lithographic viewpoint it would be possible to shrink the trench width to 2.4 µm with small adaptation of the etch depth. Main etch should not be deeper than be 46.30µm and the soft landing should add at least 6.70µm.

ACKNOWLEGEMENTS

We would like to thank Patrick Jaenen for process development and cross-sectional SEM images of photoresist patterns. We also thank Filip Beirnaert and Inge de Preter of IMEC for cross-sectional SEM images of the trenches.

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