VERIFICATION OF BACK-TO-FRONT SIDE ALIGNMENT FOR ADVANCED PACKAGING

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ABSTRACT
Leading edge consumer electronic products relentlessly drive demand for enhanced performance and small form factors. This in turn defines manufacturing requirements for all aspects of semiconductor device fabrication. As the cost of front end manufacturing continues to escalate rapidly with each new technology node, semiconductor manufacturing companies are increasing their focus on packaging technology such as silicon interposers with through silicon vias (TSV) to deliver improved performance and reduced form factor.

Lithography is one of the critical process steps that affect the final device performance and associated yield for TSV manufacturing. One of the unique lithography requirements is the need for back-to-front side alignment. Obtaining precise metrology for measuring back-to-front side overlay performance is an industry challenge. Unlike front end manufacturing where automated metrology tools are widespread, metrology options are limited for back-to-front side overlay. This paper will discuss a metrology package which has been developed to evaluate and qualify back-to-front overlay performance using the lithography tool itself. The package is unique in its capability to measure any location of the wafer and model the acquired data to provide detailed insight in back-to-front side overlay performance.

Silicon test wafers were fabricated over a range of thicknesses to evaluate the stepper self-metrology for back-to-front side overlay. The reference layer is defined in a standard damascene copper process and protected with a passivation layer. Next the wafers are flipped, bonded, and thinned to various thicknesses. Wafers were produced with coarse and fine grinds to compare with chemical mechanical polish (CMP) to assess the impact of surface interference on the alignment system of the lithography tool. Experimental back-to-front alignment metrology data is shown as a function of silicon thickness and surface finish using the lithography tool self-metrology. The accuracy of the tool self-metrology is verified independently using external infrared (IR) microscopy.

Key words: Metrology, Overlay, 3D Packaging, TSV, back-to-front side alignment

INTRODUCTION
Over the last four decades semiconductor device manufacturers and wafer foundries have utilized shrinking gate dimensions and decreasing operating voltage to enhance device performance. This approach has driven broad industry growth. However as customers transition to sub-28 nm manufacturing technology, traditional front end scaling is becoming increasingly complex with significant cost impacts. Semiconductor manufacturing companies are focusing on various packaging technologies to play an important role in delivering improved system level performance in a cost effective manner. The manufacturing approach utilizing three dimensional (3D) TSV technology alleviates interconnect delay considerations by reducing global interconnect wiring length. In addition, TSV delivers superior bandwidth performance, power management and addresses some device latency issues. Many companies have research activities in 3D TSV technology and numerous demonstration vehicles have been developed [1,2]. Some of these TSV processes sequences require the need for back-to-front alignment solutions during the lithography process step.

Interposers for packaging also require TSV technology. Devices under consideration for use with interposers include graphics processors, high-end ASICs, and FPGAs. The drivers are mainly partitioning large die, integrating single chips into a module, reducing die size where substrate density is the constraint, and the use of the interposer to minimize the stress on large die that is fabricated with extra-low-k dielectrics (ELK).

While image sensors have utilized TSV technology in mass production over the last few years, it is projected that DRAM manufacturers will begin utilizing the TSV packaging technology within several years [1,3]. Adoption of this technology by memory companies can play a significant role in driving technology adoption. However the requirements for memory manufacturers are much more

stringent and require development of improved back-to-front alignment capability.

TSV technology is the primary driver to improve IR back-to-front capability. However, other technologies can benefit from this capability. The design possibilities for MEMS, microfluidics and bio-technology devices can be greatly enhanced with the improved alignment capability and metrology examined within this study [4,5].

ALIGNMENT SYSTEM

The naming convention used in this study is that the wafer device side is the front side and the silicon side is the back side. The side facing up on the lithography tool is the back side of the TSV wafer as shown in figure 1.

Various methods have been investigated for viewing embedded lithography alignment targets [6]. The method of top IR illumination, shown in figure 1, provides practical advantages for integration with stepper lithography. Since the illumination and imaging are directed from the top, this method does not interfere with the design of the wafer chuck, and does not constrain where alignment targets can be located on the wafer.

The top IR alignment method illuminates the alignment target from back side using an IR wavelength that can transmit through silicon (shown as light green in figure 1) and the process films (shown in blue). For this configuration the target (shown in orange) needs to be made from an IR reflective material such as metal for best contrast. The alignment sequence requires that the wafer move in Z in order to shift alignment focus from the wafer surface to the embedded target.

The lithography system used in this investigation has a top IR alignment system that supports back-to-front side alignment applications. The back-to-front side alignment or dual side alignment (DSA) application was originally developed for CMOS image sensor applications [3]. This application required alignment to embedded metal targets below silicon, and the system was designed to achieve back-to-front side overlay of less than 2.0 µm (|mean| + 3sigma) over a full 300mm wafer. However, a large portion of this budget is consumed by the error uncertainty of the back-to-front metrology.

Unlike many front side alignment systems which view the wafer through the projection lens (TTL), the DSA alignment system views the wafer in an off-axis configuration. Therefore the calibrated offset between the exposure and alignment systems is maintained using a common stage fiducial that is measured by both the DSA and TTL alignment systems. Note that the DSA alignment camera is in a fixed position. The wafer stage on the stepper moves in X and Y to enable alignment at any location on the wafer, and the wafer stage also provides the range of Z travel to allow focus on both top surface targets and embedded targets across the practical range of silicon thicknesses.

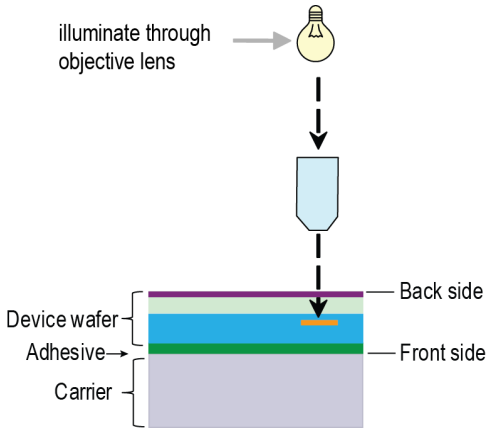


Figure 1: Off axis alignment configuration with infrared illumination and imaging from above the wafer. This configuration is the most flexible, providing access to the entire wafer for target alignment.

METROLOGY

The wafer processing sequence consists of off-axis alignment of the embedded targets on the lithography tool followed by an exposure of the reticle pattern to form resist patterns on the back side. However finding suitable methods for evaluating back-to-front side overlay performance with available metrology is a challenge. Typical registration metrology systems measure topside planar structures, and for initial DSA investigations various overlay tests were constructed to accommodate this metrology restriction [7]. The Single Pass overlay test, which uses monitor wafers with an etched pattern at the surface, allows detailed characterization of the off-axis alignment system. The Single Pass overlay test is very useful for monitoring performance, but this test does not view targets through silicon and does not require a Z move between alignment and exposure [6,7]. The Double Pass embedded overlay test addresses this shortcoming by aligning to embedded targets and forming resist patterns at the top surface using two separate passes at 0 and 180 degree orientation respectively. The overlay between the two passes can then be measured using a conventional topside metrology system [6,7] The Double Pass test provides useful information about mean performance and stability. However this test cannot be used for detailed overlay analysis because linear modeling terms cancel out in the double pass operation. The limitations of the Single Pass and Double Pass overlay tests can only be address by direct measurement of back-to-front alignment. Direct metrology provides the overlay data required for effective process monitoring and overlay optimization.

To eliminate the inherent restrictions in topside planar metrology, a direct back-to-front side registration metrology package was developed to run on the lithography system, utilizing the off-axis IR alignment system. This metrology method incorporates separate focus offsets and separate pattern recognition models to achieve optimum pattern capture and localization for each pattern. The implementation includes utilities for recipe management;

and is capable of measuring many sites across the wafer and on multiple wafers. The new metrology package enables realistic testing of back-to-front alignment.

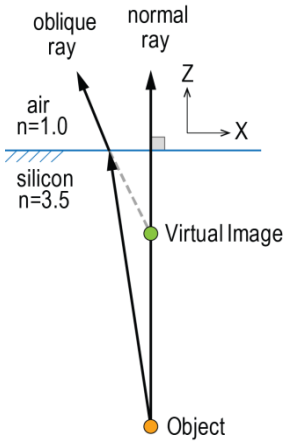


Figure 2: Ray trace of the principal ray shows that the apparent target position viewed from the air side appears at different Z position, but has the same XY position as the actual target position.

To understand the potential issues affecting back-to-front metrology, a simple model for imaging an embedded target under the silicon can be constructed from ray tracing analysis, as shown in figure 2. Viewed from the air side, light refraction at the air/silicon interface makes the virtual image (green) appear higher in Z than the actual object position (orange). This estimation problem does not exist in the lateral direction: the virtual image and object positions are the same in X and Y. Therefore the virtual alignment target provides a stable reference for overlay metrology.

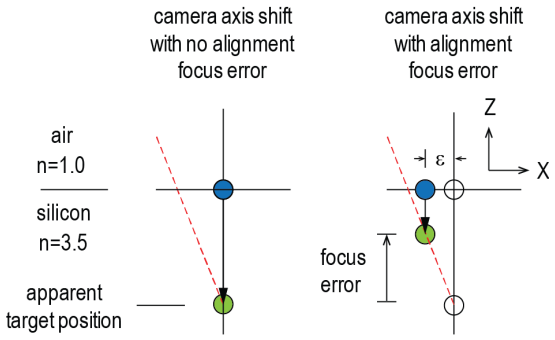


Figure 3: Tilt of the alignment system can create a lateral error (ε) in captured position if there is an alignment focus error. Focus error will cause the perceived image position to shift along the axis of the alignment system shown as a dotted line. Arrow shows the Z shift translation from the surface position to the corresponding alignment target position.

There are several potential error sources that need to be considered in the design of the metrology system. If the principal ray of the alignment system is tilted from the wafer normal, then this pointing error in the alignment system can produce a lateral measurement error (ε) if the alignment target is not viewed at best focus as shown in figure 3. Therefore maintaining best focus is important in minimizing the effects of an alignment system pointing error. Focus is generally well controlled in a lithography system since errors in focus will also affect the image appearance and localization by the pattern recognition algorithm.

Another potential source of registration error is tilt of the Z-axis. An angular error of the Z-axis results in a lateral translation (ε) proportional to the size of the Z move. This can have a large effect when there is a large Z shift from the alignment focus position to the exposure focus position, as shown in figure 4. Note that this error cancels out in the new back-to-front side measurement method since the same sequence is used for both wafer alignment and metrology. Therefore this error needs to be independently characterized to verify that it is not a significant effect. This error can be effectively measured with the double pass test [6].

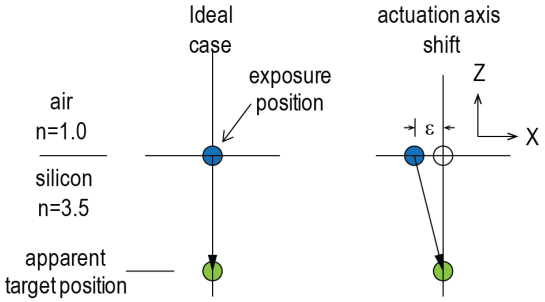


Figure 4: Diagram showing the effect on Z-axis tilt on overlay. A Z-axis tilt shifts the target during the Z-axis move from the surface position to the corresponding alignment target position.

EXPERIMENTAL METHODS

The lithography system used for back-to-front side alignment and metrology is an Ultratech AP300 DSA stepper. The system has a 0.16 NA, 1X Wynne-Dyson projection lens design with broadband ghi-line Hg illumination [8,9]. The stepper is used in high volume advanced packaging applications and provides a stable platform for DSA operation. In this investigation a new back-to-front side metrology capability is evaluated.

The previous stepper self metrology package was designed for all metrology targets to be at the same Z height. This results in metrology targets from one level being out of focus compared to the other level when measuring DSA structures as shown in Figure 5. The new back-to-front side metrology package used in this study provides flexibility to measure targets at different Z heights with different designs at each level as shown in figure 6. This requires sequential measurement of two patterns at each measurement site and the ability to specify focus offset and pattern recognition

model for each pattern. A precision mechanism in the wafer stage provides Z travel normal to the wafer, which is required in order to minimize registration error as discussed in the Metrology section of this paper. Since the metrology package uses the same target capture mechanism as the alignment system, the error analysis has similar terms. For example, since the Z travel angle is common to alignment and metrology operations, the effect of this angle cancels and cannot be characterized by this method.

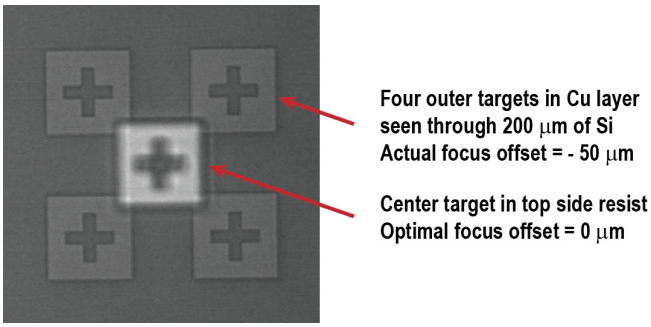


Figure 5: The orginal SSM measurement clover leaf target expects all five sub targets in the same focal plane. This approach does not work for DSA applications: top side and embedded targets are in different focal planes.

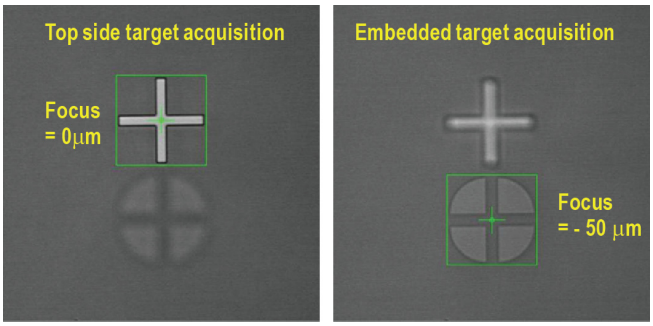


Figure 6: New Stepper Self Metrology for DSA changes focus between acquisition of top side and embedded targets. The embedded target is 200 μm into the Si. Note that light refraction at the air/silicon interface makes the virtual image appear higher in Z (-50 μm) than the actual object position (-200 μm).

Monitor test wafers for topside overlay baseline testing were prepared. The first pattern level was created using an ASML PAS5500/750 deep UV scanner with a specially designed mix-and-match test reticle containing alignment targets and various metrology structures. These patterns were etched 500 nm into the silicon surface to make artifact wafers, Baseline monitoring for the single pass test can be performed using metrology for topside planar structures. These wafers were used to calibrate the off-axis alignment to a calibrated reference [10].

The embedded target test wafers were prepared using a copper damascene process. A dielectric layer consisting of 250 nm of SiO_2 was deposited followed by an etch-stop layer and 600 nm of SiO_2. Then an ASML PAS5500/750 deep UV scanner was used to image a first pattern level with a specially designed mix-and-match reticle. After etching the 600 nm SiO_2 layer, 1000 nm of copper was deposited to fill the trenches and Chemical Mechanical Polish (CMP) was used to expose the underlying oxide, leaving a flat surface with copper filled trenches. This was covered by a SiO_2 passivation layer.

The copper damascene wafers were inverted and glued to a silicon carrier. The wafers were thinned using a grinding system to four Si thicknesses (50, 100, 200 and 300 μm). The last step was polishing the surface by CMP to remove surface damage leaving an optically smooth surface. The TTV (Total Thickness Variance) of the wafers was measured to be below 3 μm. A drawing of the wafer cross section is shown in figure 7. Some wafers were also prepared and left un-polished to evaluate the impact of the coarse and fine grinding scratches on the embedded target alignment performance.

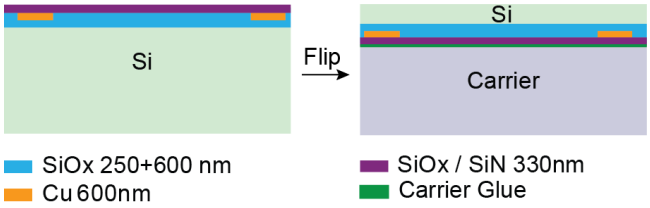


Figure 7: Cross section of test wafers with embedded damascene Cu targets. Wafers are inverted, glued to a carrier, and then the silicon is thinned and polished.

A mix-and-match test reticle designed to match the PAS5500/750 patterns was used on the AP300 for printing a second level matching pattern for back-to-front registration testing. The metrology structure compares the embedded copper damascene pattern to the topside resist pattern.

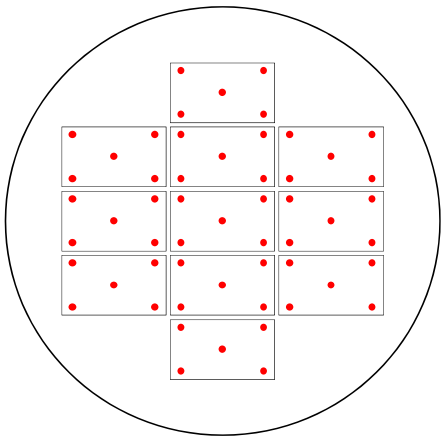
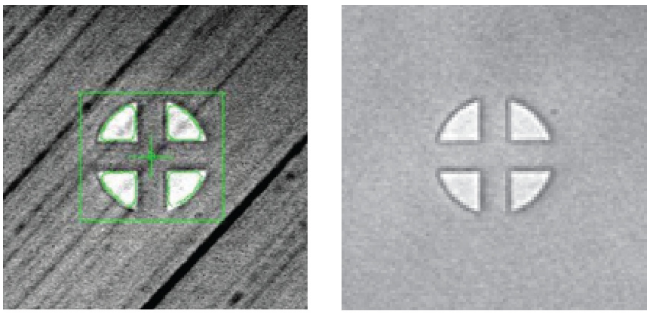


Figure 8: Metrology sampling plan on 200 mm wafer. Dots in the wafer map denote measurement locations.

The stepper self metrology sampling plan is shown in figure 8. It consists of five sites per field in eleven fields for a total of 55 sites across the wafer. The metrology measurements

can be collected quickly which allow a large number of measurements for inter and intrafield characterization.

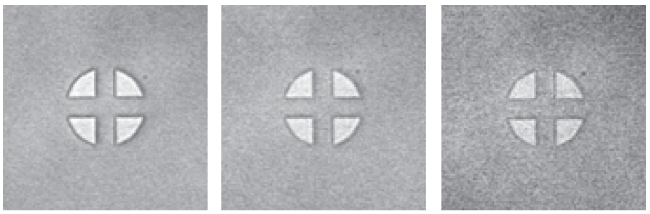
The polishing sequence consists of a grind operation followed by CMP. To study the effect of polishing quality, wafers were produced with coarse grind and fine grind to compare with the CMP wafers. Photos of coarse and CMP images are shown in figure 9. Severe scratches are visible on the coarse grid wafers while the CMP provides virtually perfect images. Since the visible surface scratches can obscure targets depending on where they fall, target enhancement and backup strategies can be used to eliminate alignment risk. However, the target image capture and overlay performance was good for all three finishes.



(a) Coarse grind (b) CMP polished

Figure 9: DSA camera view of (a) wafer after coarse grinding, (b) wafer after grinding and CMP. The wafer is 100 μm thick silicon.

The effectiveness of the IR DSA camera for viewing embedded metal targets is shown in figure 10 for 100, 200, and 300 μm thick silicon. Image quality for alignment can be maintained across this practical range of silicon thickness. Even at the thickest 300 μm thick film the target image quality was good and no problems were observed for alignment capture or overlay performance.



(a) 100 micron (b) 200 micron (c) 300 micron

Figure 10: Images of DSA targets through three thicknesses of Si.

To provide an independent check of the accuracy of the embedded wafer alignment, an Olympus LEXT OLS4000 laser scanning infrared confocal microscope with 300 mm motorized stage was used. This microscope uses a Z move to capture surface and embedded images, and manual analysis of 0 and 180 degree orientation measurements was performed on the composite images. The two orientations were used to calibrate a tool bias for each individual wafer. The automatic mode was not used since the intensity variation of the two image positions prevented reliable measurement. Manual data collection and analysis greatly limit the amount of data that can be collected. Measurement sample for each wafer consists of five fields with five sites per field for a total of 25 sites.

For embedded target measurement, a particular challenge for accurate TIS measurement is to perform a pure 180 degree rotation about the wafer normal. This is a challenge for most microscope systems because rotation of the wafer chuck by 180 degrees typically changes the wafer tilt relative to the optical axis. To calculate a correction for tilt on the microscope, the relative tilt of a flat wafer at zero and 180 degree chuck rotation was measured by mapping Z-height readings at best focus at several positions across the wafer. This tilt correction method assumes that the measured tilt versus chuck orientation repeats for all wafers. Obtaining a consistent wafer tilt is not a problem for the stepper measurement since the global tilt compensation sets the wafer tilt to the same reference during each wafer cycle.

RESULTS AND DISCUSSION

Preliminary testing was done to verify that metrology data collected on the off-axis IR camera matches data measured with the previous method using the on-axis TTL alignment system. The two methods closely match and slight differences were attributed to the specific offsets in the different pattern recognition models used for each test. An attempt to measure tool induced shift (TIS) was unsuccessful due to by the asymmetry in the target design shown in figure 11 [10]. Future plans call for evaluating TIS using a reticle set containing an appropriate structure.

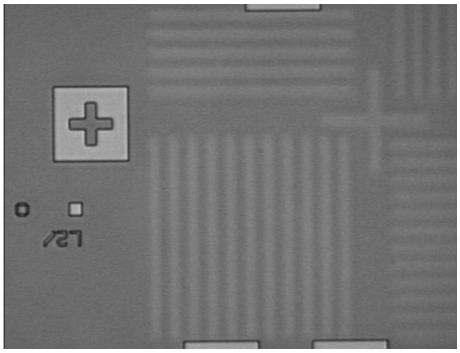


Figure 11: View from off-axis camera of resist feature (left cross in box) in focus and embedded metal mark under 200 μm thick silicon which is out of focus. Focus offset is needed to get the embedded mark in proper focus for measurement. Note that the large offset between marks and the non-symmetric nature of the embedded mark prevented reliable TIS measurement from this structure.

For back-to-front side alignment, mean versus silicon thickness data from double pass testing are shown in figure 12, and data from the LEXT microscope for the same wafers are shown in figure 13. Although the measured mean variation is not significant for the current design overlay requirements, this is a potential area for future improvement. The two measurement methods suggest a

small slope in X mean versus silicon thickness; however there is significant uncertainty in these estimates based on the data sample size. Since the silicon thickness correlates to the run time parameter of alignment focus offset, the measured slopes can be incorporated into the run time lithography system calibration to null out the effect of silicon thickness on means. Additional data collection is required to establish a reliable calibration for the system.

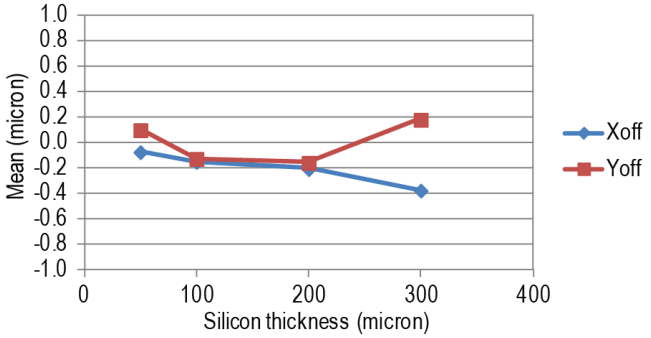


Figure 12: Plot of mean versus silicon thickness for double pass test.

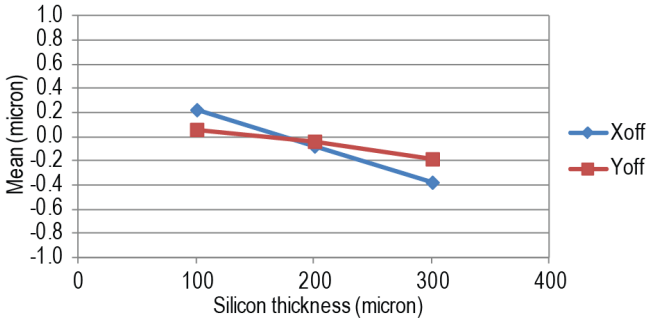


Figure 13: Plot of mean versus silicon thickness for LEXT microscope measurement.

DSA wafers with silicon thicknesses of 50, 100, 200 and 300 µm were aligned and exposed. The same off-axis alignment system was used for metrology. A plot of mean versus silicon thickness is shown in figure 14. Back-to-front overlay means are not significantly affected by silicon thickness. The results were calibrated using a fixed offset to best match the double pass result for 100 and 200 µm thick silicon. This calibration accounts for errors such as pattern training offset.

A plot of three sigma versus silicon thickness is shown in figure 15. Back-to-front three sigma is not significantly affected by silicon thickness 100 µm or greater. However the 50 µm thickness exhibited a large three sigma.

The linear terms in the overlay analysis reveals that the 50 µm thick silicon wafers have a large isotropic (17 ppm) intra-field scaling compared to thicker wafers. This scaling is suspected to come from distortion of the thin silicon film during the bonding process. Further study with more wafers having less than 100 µm silicon thickness is necessary.

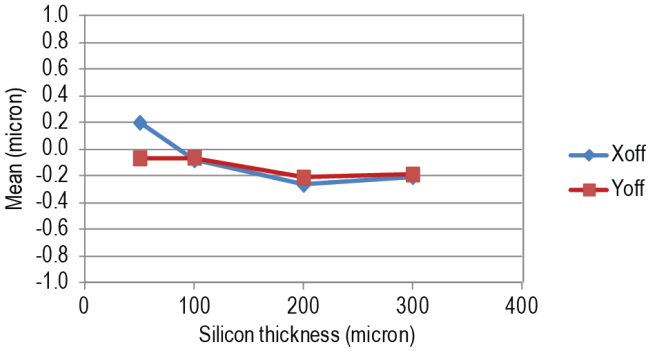


Figure 14: Plot of mean versus silicon thickness for back-to-front side measurement.

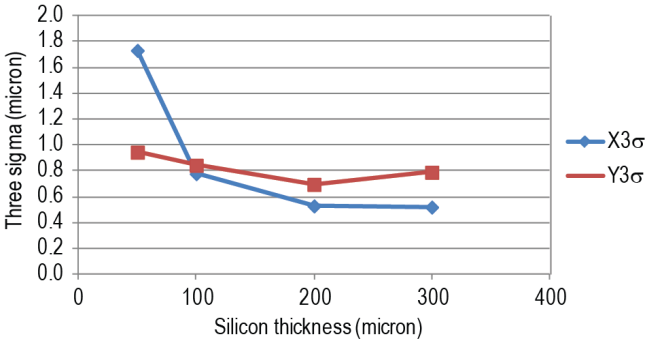


Figure 15: Plot of three sigma versus silicon thickness for back-to-front side measurement. Increased variation in X for the 50 µm thick silicon is due to a larger scaling of the wafer pattern, suspected to be caused by distortion of the thin silicon film during the bonding process.

Three different grades of surface polishing were investigated. The three polishing grades, in order of increasing surface quality, are coarse grind, fine grind and CMP. In extreme cases the surface scratches can interfere with the capture of particular targets; however miscapture can be avoided through proper setting of pattern capture criteria and the use of backup targets [7]. Figure 16 shows a plot of three sigma versus silicon thickness for front-to-back side measurement for 200 µm silicon and various polishing techniques. The three grades of polish give similar results for three sigma.

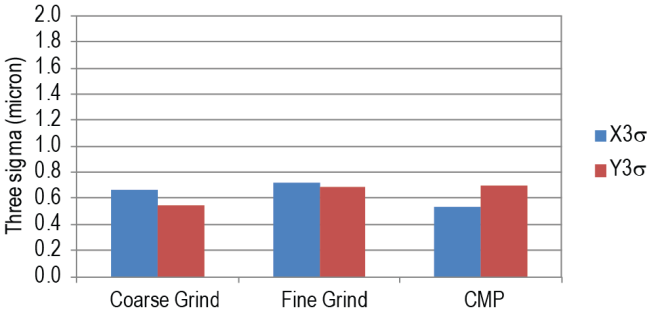


Figure 16: Plot of 3-sigma versus polishing technique for 200 µm thick silicon.

CONCLUSIONS

A new back-to-front metrology method was developed to provide direct feedback for overlay optimization and monitoring. It provides flexibility to measure targets at different Z heights with different target designs.

Silicon test wafers have been fabricated with a range of silicon thicknesses and surface polish to evaluate the stepper self-metrology for back-to-front side overlay. Mean versus silicon thickness data using the self metrology double pass test was compared with the LEXT microscope metrology. The level of variation is not significant for current design overlay requirements.

Using the new metrology method, back-to-front overlay means are not significantly affected by silicon thickness. Back-to-front three sigma is not significantly affected by silicon thickness 100 μm or greater. However the 50 μm thickness exhibited a large three sigma due to isotropic scaling. This scaling is suspected to come from distortion of the thin silicon film during the bonding process, and further study with more wafers having less than 100 μm silicon thickness is necessary.

Three different grades of surface polishing were investigated. The quality of surface polish did not affect the overlay performance. However severe surface scratches can potentially obscure targets requiring that backup target strategies be used for wafer alignment mapping.

Ongoing work will look at collecting more DSA overlay data to improve the lithography system calibration to null out the effect of silicon thickness on means. A revised reticle set with symmetric targets will be evaluated for TIS measurement. Additional work is required to address the observed TIS error with the infrared microscope due to variation of wafer tilt relative to the optical axis.

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