Veeco

Precision Surface Processing

Effective Post-TSV-DRIE Wet Clean Process for Through Silicon Via Applications

Laura Mauer, John Taddei, John Clark, Kenji Nulman

Veeco Precision Surface Processing
Horsham, PA 19044
lmauer@veeco.com

Stephen Olson, Victor Vartanian, Michael Hatzistergos

SUNY Polytechnic Institute
Albany, NY 12203
solson@sunypoly.edu

***Abstract*—Deep Reactive Ion Etch (DRIE) processes used to form Through Silicon Vias (TSVs) achieve high aspect ratios by depositing polymer on the vertical sidewalls of the features. This polymer material must be removed before other materials (including dielectric liner, Cu barrier, and Cu) are deposited in the TSVs. Clean processes adapted from Cu damascene integration flows use a combination of oxygen ash and wet clean to remove the residual photoresist and sidewall polymer to prepare the inside surface of the TSV for subsequent films. In this work, we show the performance of a cleaning process utilizing exclusively wet methods. The removal of both the photoresist and sidewall polymer is accomplished with a combination of soak and high-pressure spray process using an environmentally friendly chemistry. This reduces the total number of process steps, leading to a reduction in overall cost. Previous work has shown that physical analysis, including SEM, EDX, and Auger, as well as electrical testing, are required to determine cleanliness. This study focuses on electrical testing to qualify the performance of the wet-only clean. Electrical testing allows measurement of the aggregate behavior of up to thousands of TSVs. In-line Test (ILT) uses capacitance, leakage, and conductance to determine the performance of the M1 and TSV dielectric liners. Dielectric breakdown voltage measured using a Voltage Ramp Dielectric Breakdown (VRDB) method is used to test the reliability of the TSV dielectric liner. In this work, the cleaning performance was evaluated using two via diameters (2 and 5 microns) and two aspect ratios (10:1 and 20:1).**

Keywords-Through Silicon Via, TSV, clean, Auger

I. Introduction

Through-Silicon-Via (TSV) technology allows electrical connections to be made vertically through a chip. When integrated into a design, this technology can be used to reduce the interconnect length, reduce the package size, and increase the bandwidth between chips.

The trade-off for forming connections vertically within the die is reduced area to build logic devices. Micron-sized TSVs are very large compared to the size of transistors. The Si immediately adjacent to the TSVs may not be usable due to stress from the large volume of metal. This creates a keep-out zone around the TSVs. Scaling the diameter of the TSV reduces the surface area lost to the TSVs and reduces the size of the keep-out zone [1]. Scaling the diameter also scales the depth of the TSV. In cases where a minimum die thickness is required for handling, higher aspect ratio etching processes are required to scale the lateral dimension of the TSV.

Deep Reactive Ion Etch (DRIE) processes achieve high aspect ratios by depositing polymer on the sidewall of the TSV during the etch process. This protects the sidewall, allowing the etch to proceed only at the bottom of the feature. In the Bosch DRIE etch process, this is accomplished by alternating steps of aggressive etch followed by fluoropolymer deposition. Various clean processes are used to remove this polymer material from the TSV.

In this work, we show the performance of a new wet clean process using exclusively wet methods. The performance is evaluated using electrical testing and verified using physical metrology.

II. Experiment Description

A. Clean tool and process

A successful process requires a combination of the appropriate chemistry and equipment. Dynaloy developed Dynastrip™ DL9150 which is a non-TMAH-containing multi-purpose post-Bosch DRIE process fluorinated residue remover. This formulation has environmental, health, and safety advantages due to its lower toxicity profile compared with common TMAH-containing products. It combines efficient and effective polymer dissolving technology with metal compatibility for use in integrated processes. Preliminary evaluation of Dynastrip DL9150 for TSV cleaning has been reported previously [2]. In this study, Dynastrip DL9150 was used in a Veeco PSP WaferStorm® combination immersion batch soak and single-wafer spray solvent processor. The combination of two process techniques (immersion batch soak and single-wafer spray) in a single system provides unique capabilities for photoresist strip and polymer removal processes.

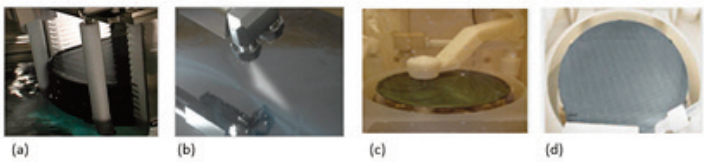

Figure 1. Process sequence (a) heated solvent immersion (b) heated high-pressure fan spray (c) rinse (d) spin dry

Each wafer is soaked under precisely controlled conditions in a heated, recirculating, solvent immersion bath with a nitrogen environment. Sequencing is based on the downstream process times, assuring each wafer is soaked the same length of time. With the appropriate chemistry, the soaking time allows for dissolution of the photoresist and removal of the sidewall polymer coating.

Following the soak, the solvent-wet wafer is transported to a single-wafer spin process station for complete removal of residual photoresist and sidewall polymer. The use of a high-pressure chemical fan spray enhances the removal of residuals. The rinsing process ensures the wafers are completely clean and particle free.

B. Process flow

The TSV clean was integrated into CNSE's (College of Nanoscale Science and Engineering) standard flows for forming 5x50 (5.5 µm diameter, 50 µm deep) and 2x40 (2 µm diameter, 40 µm deep) TSVs. TSVs are fabricated on 300 mm, lightly p-doped Si wafers. A short-loop demonstration flow is used to investigate only the properties of the TSVs. The process flow is shown in Figure 2. A TEOS (Tetraethyl orthosilicate) film is first deposited on the Si wafer (a). This film simulates films that would likely be included in a TSV-mid integration. The TSVs are patterned using standard (Middle Ultraviolet) MUV photolithography. A Bosch-type etch is used to etch Si from the TSV hole (b). The TSV is lined with an oxide formed by an Ozone/TEOS thermal chemical vapor deposition process (c). Cu barrier and seed films are deposited and Cu is electroplated into the TSV (d). The TSV-Cu overburden is removed using CMP and a single damascene metal is formed above the TSVs (e).

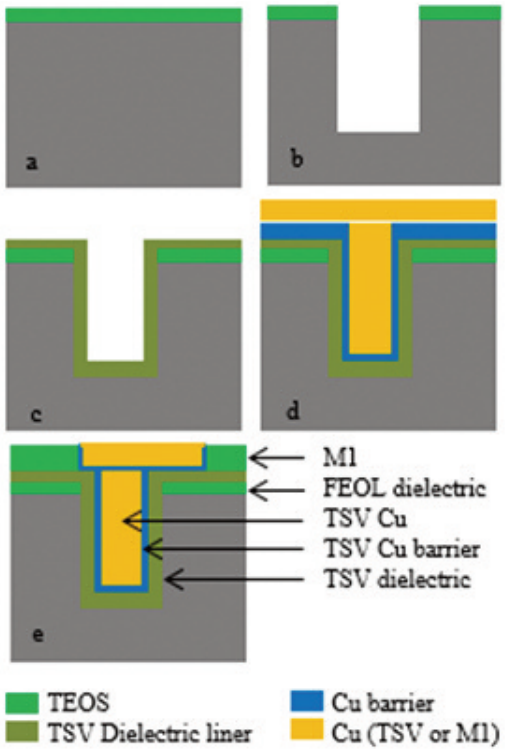

Figure 2. TSV Fabrication Flow

The Veeco wet clean process is inserted between step (b) and (c) of the process flow in Figure 2. A more detailed description of this process and the experimental split is shown in Figure 3. The RIE process has 3 steps. The first two steps open the oxide on the surface of the wafer and etch the Si. The third step is an oxygen ash used to remove the photoresist. Our standard process uses dilute HF and NH4OH:H2O2 after the DRIE process to clean the TSVs. Experiments were designed that used the new Veeco wet clean to replace the existing dHF/NH4OH:H2O2 wet clean, as well as to replace the ash and existing wet clean. Removing the ash step reduces the RIE process time by 33%. POR is Process of Record.

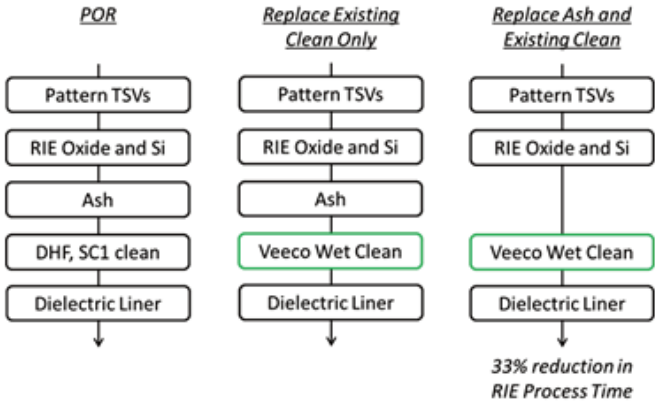

Figure 3. Clean integration

C. Electrical Test

An electrical test was used to evaluate the performance of the clean process. **Error! Reference source not found.** shows a schematic diagram of the test setup. Arrays of TSVs are connected to bond pads on the front surface of the wafer. Voltage is applied between the TSVs and the bottom of the wafer. Using this configuration, we measure leakage current to the substrate at low voltages, then ramp the voltage in a step pattern to find the voltage where the TSV dielectric breaks [3]. In our standard configuration the positive voltage is applied to the Cu TSV. We use optical illumination to generate minority carriers and add a delay to allow the TSV-oxide-Si capacitor to charge [4].

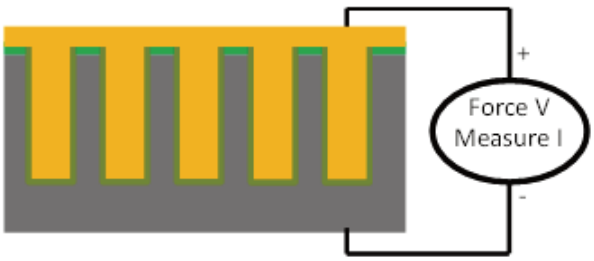

Figure 4. Electrical test setup

III. Results and Discussion

The methodology in section II was used to evaluate the performance of the clean process. Four lots were processed, including 2 µm and 5.5 µm diameters, with and without the ash step. Recipe splits were set up around soak time and rinse process. The first step in the Veeco clean process is a soak in Dynastrip™ DL9150. The soak station is set up as a wet-buffer, operating with a first-in first-out methodology. This allows the process throughput to be limited by the following steps when in continuous operation. Soak times from 1800 to 3600 seconds were used. The wafers were rinsed using DIW with megasonic agitation or SC1 with high-velocity spray, with both followed by a DIW rinse and spin dry. The split table for the four clean experiments is shown in Table I. For the 5x50 lots, wafers were processed with no wet clean as well.

Table I. TSV Clean Split Table

		Number of Wafers			
		5x50		2x40	
Soak Time (s)	Rinse	Ash	No-Ash	Ash	No-Ash
1800	Mega DIW	3	3	3	3
	SC1	3	2	-	3
2700	Mega DIW	3	1	-	-
	SC1	3	2	-	-
3600	Mega DIW	3	3	3	3
	SC1	3	3	3	2
POR		5	3	6	3
No clean		2	2	-	-

A. 5x50 TSV Clean

The 5x50 TSV wafers processed through TSV etch-with-ash step were cleaned using the recipe table in Table . Three different soak times, each with both rinse processes, were investigated. Variations were run a total of three times In addition, five wafers were processed in parallel using our POR, and two wafers were processed without a wet clean.

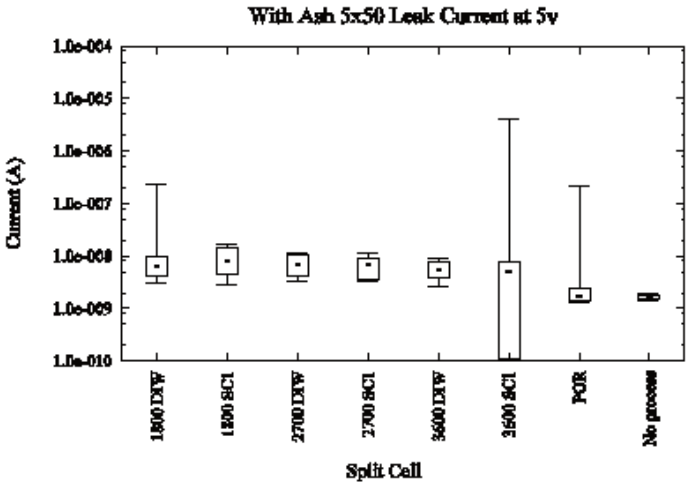

Figure 2. 5x50 with-ash TSV leakage current at 5v

Figure 2 shows the leakage current from the TSVs to the back side of the wafer at 5v. Each split cell is shown using a bar and whisker plot. The whisker shows the extreme values. The bar shows the 10 to 90 percentile range. The center line is the median value. Thirty-two dies were measured on each wafer. All wafers for a split cell are combined into the bar and whisker.

The split cell without a wet clean performed similarly to the wafers cleaned using our standard SC1 and HF clean. This shows that the polymer in the TSV is removed primarily by the ash process. The wafers cleaned at Veeco all show a small increase in leakage current compared to the standard process wafers. Soak time and rinse process did not affect the leakage current measurement in a repeatable way.

The dielectric breakdown was measured by ramping the voltage to 100v in 5v steps. The graph in Figure 3 shows the breakdown voltage. The whisker shows the extreme values, the box shows 10 to 90 percentile, and the center line is the median. Twelve dies are measured on each wafer. For these graphs, breakdown current is defined as 1 µA. The measurement only goes as high as 100 volts. This is not sufficient to break the dielectric in most cases.

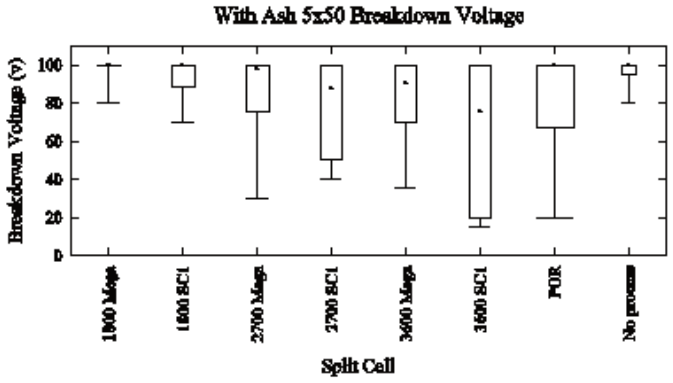

Figure 3. Dielectric breakdown voltage for 5x50 with ash lot

It is unclear why the POR processed wafers had some dies fail at low voltages. Shorter clean processes had fewer dies that failed at low voltages.

A similar experiment was performed for 5x50 TSVs without the ash step after the TSV etch. Leakage at 5v is shown in Figure 4. This lot had a different number of wafers in some split cells due to design and loss in processing. The width of the bars represents the number of wafers in the dataset.

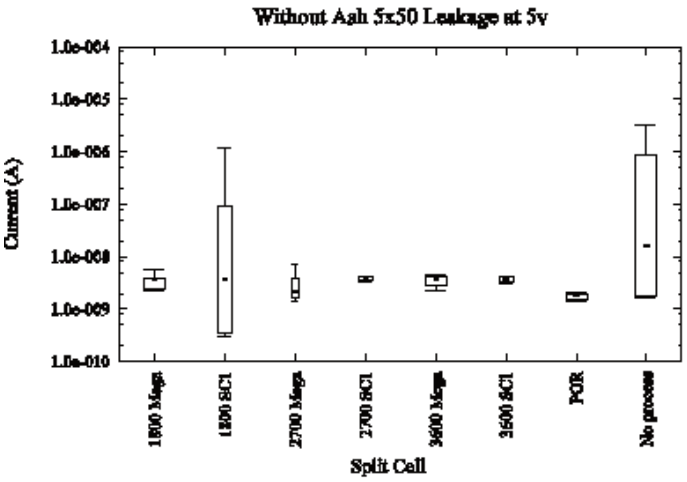

Figure 4. 5x50 no-ash leakage current at 5v

The higher leakage current with no clean further confirms that the ash process is primarily responsible for removing RIE polymer from the TSV. The Veeco clean had average leakage current approximately the same as the POR processed wafers, however there was a larger spread in the data. This shows that the clean is effective at removing the polymer normally removed by the ash step. Cleaning time did not affect the median leakage value. The larger spread in the data for the 1800-second process shows that this may be close to the process window edge.

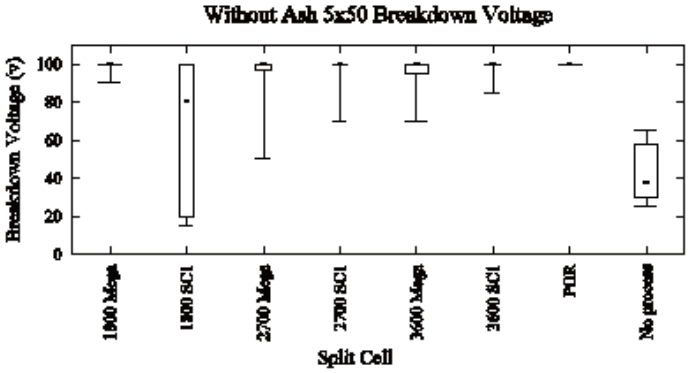

Figure 5. 5x50 without ash breakdown voltage

Breakdown voltage is shown in Figure 5. Breakdown voltage was greater than 100v for all dies in the POR split cell. All dies on wafers without a clean process failed before 60v. Wafers cleaned at Veeco have some dies fail below 100v, with a trend toward better performance as clean time increased.

B. 2x40 TSV Clean

A similar cleaning experiment was performed to show the performance of the Veeco clean on 2-µm diameter TSVs. Leakage current at 1v is used as a metric for the 2x40 dimension. Leakage current for the with-ash 2x40 wafers is shown in Figure 6.

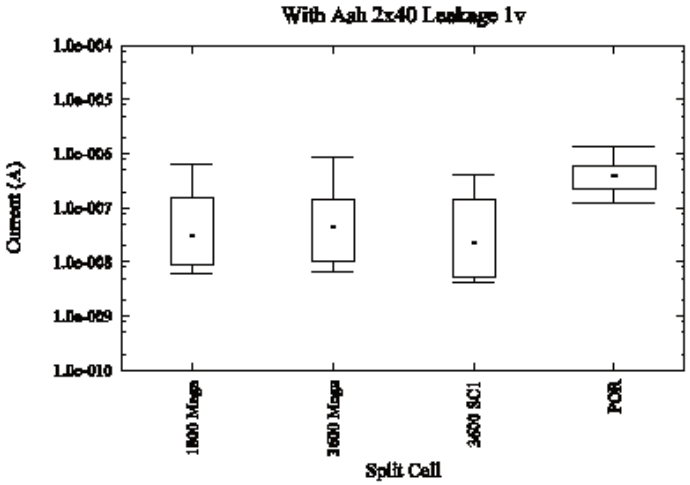

Figure 6. 2x40 with-ash TSV leakage current at 1v

The wafers cleaned at Veeco had slightly better performance, suggesting that there was some material to be removed. VRDB measurements in Figure 7 also show higher breakdown voltages for the wafers cleaned at Veeco.

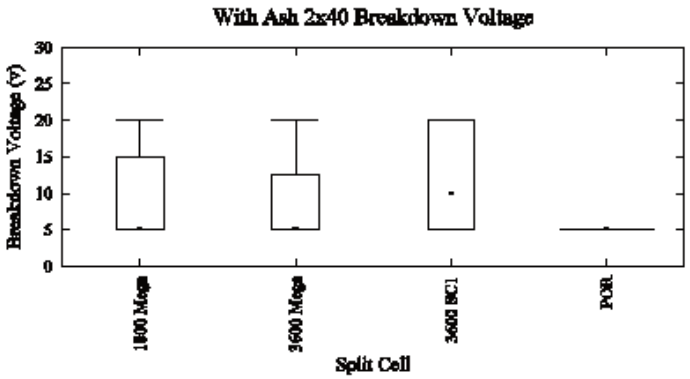

Figure 7. Breakdown voltage for 2x40 with-ash wafers

Leakage data for no-ash 2x40 wafers is shown in Figure 8. The wafers cleaned at Veeco had similar leakage as the POR wafers, with outlying dies having lower measured current. Soak time did not have much effect on the leakage current.

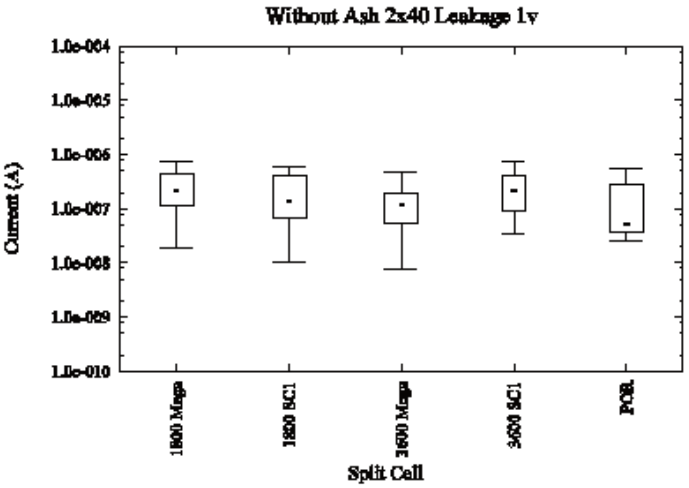

Figure 8. 2x40 no-ash TSV leakage current at 1v

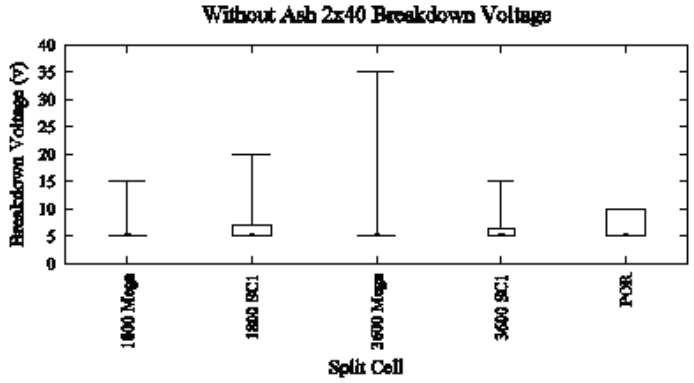

Figure 9. 2x40 without ash breakdown voltage

Breakdown voltage for the 2x40 no-ash lot is shown in Figure 9. Most dies had breakdown at 5v or less. Outlying dies show a trend toward better performance with increasing clean times.

IV. Clean Process Metrology

Error! Reference source not found. shows SEM images of 5x50 TSVs before and after the Veeco clean process. All of the photoresist has been removed from the surface of the wafer. There is no residual material or damage to the TSV.

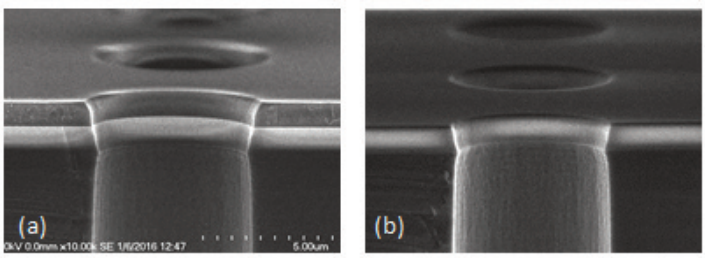

Figure 13. SEM images (a) before clean (B) after clean

Auger Electron Spectroscopy (AES) was employed to examine the presence and composition of residue on the TSV sidewalls. An AES680 from Physical Electronics with 1E-10 Torr base pressure, equipped with a cylindrical mirror analyzer and a field emission gun provided the necessary resolution to probe the desired TSV regions. Various depths were examined by cleaving the specimen through the TSVs and introducing it in the AES system tilted at 90 degrees for cross-sectional imaging and analysis.

The 5x50 and 2x40 TSV wafers were cleaned using the 1800 second, SC1 recipe. Sample wafers were measured before and after the cleaning process. Due to the destructive nature of the sample preparation, different wafers are used for the before and after measurements. Process conditions for the two wafers were identical.

Table II. AES Measurement

Atomic % Values	5x50				2x40			
	Carbon		Fluorine		Carbon		Fluorine	
	Pre	Post	Pre	Post	Pre	Post	Pre	Post
Top	18.5	12	0.5	-	68.5	37	2	-
Middle	12	12	0.5	-	63	31	1	-
Bottom	10.5	12	-	-	58.5	17	1	-
Off TSV	4	9	-	-	5	14	-	-

The AES signal was analyzed for the presence of Si, O, C, and F. The AES findings are summarized in Table II. Measurements were acquired from three locations within the vias (top, middle, and bottom). Spectra on freshly cleaved silicon next to the TSV (Off TSV) shows the background levels. The AES measurements show the Veeco cleaning process removes all detectable fluorine, and reduces the C concentration.

V. Discussion and Conclusions

Electrical and physical analysis show the Veeco wet clean removes both the photoresist and sidewall polymer residues from the TSVs. The Veeco wet clean process has demonstrated results based on leakage current and dielectric breakdown voltage that are similar to the POR while eliminating the ash, which is a significant portion of the plasma process. The additional spread in the data represents larger wafer-to-wafer and within-wafer variation, which may be attributed to the manual nature of the demo tools as well as the additional time required to ship and return the wafers from the demo site. Overall, the Veeco wet clean process has shown the feasibility equivalent electrical result and cost reduction by eliminating the plasma ash.

ACKNOWLEDGMENTS

We would like to thank Diane Scheele and Kim Pollard at Dynaloy for their technical support and guidance with the use of Dynastrip for TSV Clean. We would like to thank John Mucci of CNSE for his help developing TSV etch recipes for this work. We would like to acknowledge Susan Wiand of CNSE for help with SEM imaging.

REFERENCES

[1] J. P. Gambino, S. A. Adderly, J. U. Knickerbocker, "An overview of through-silicon-via technology and manufacturing challenges", Microelectronic Engineering, Volume 135, 5 March 2015, pp. 73-106.

[2] K. Pollard, M. Guo, R. Peters, M. Phenis, L. Mauer, J. Taddei, R. Youssef, J. Clark, "Efficient TSV Resist and Residue Removal in 3DIC," IMAPS Device Packaging Conference, 2014.

[3] Victor Vartanian et al., "Short Loop Electrical And Reliability Learning For Through Silicon Via (TSV) Mid-Wafer Front-Side Processes", International Symposium on Microelectronics: Fall 2014, Vol. 2014, No. 1, pp. 000794-000803.

[4] K. Hummler et al., "TSV and Cu-Cu direct bond wafer and package-level reliability," Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd, Las Vegas, NV, 2013, pp. 41-48. doi: 10.1109/ECTC.2013.6575548.